WHAT IS CLAIMED IS:

1. An electro-luminescence device, comprising:

an electro-luminescence element; and

a thin film transistor electrically connected to the electro-luminescence element, the thin film transistor comprising:

a gate electrode formed over a substrate;

an insulating layer formed over the gate electrode;

a first semiconductor pattern formed over the insulating layer;

an etch stop layer formed over the first semiconductor layer;

a second semiconductor pattern formed over the etch stop layer at one side of the etch stop layer;

a third semiconductor pattern formed over the etch stop layer at another side of the etch stop layer;

a source electrode formed over the second semiconductor pattern; and

a drain electrode formed over the third semiconductor pattern.

2. The electro-luminescence device of claim 1, wherein the electro-luminescence element comprises:

an anode electrode;

a light emitting layer formed over the anode electrode; and

a cathode electrode formed over the light emitting layer.

3. The electro-luminescence device of claim 2, wherein the anode electrode is electrically connected to the drain electrode of the thin film transistor.

4. The electro-luminescence device of claim 2, wherein the light emitting layer is an organic light emitting layer.

5. An electro-luminescence device, comprising:

a gate bus line extending in a first direction over a substrate;

a data bus line extending in a second direction over the substrate;

a power supply line extending parallel to the data bus line over the substrate;

a switching transistor electrically connected to the gate bus line, the switching transistor comprising:

a first gate electrode extending from the gate bus line;

a first semiconductor pattern formed over the first gate electrode;

a first etch stop layer formed over the first semiconductor pattern;

a second semiconductor pattern formed over the first semiconductor pattern at one side of the first etch stop layer;

a third semiconductor pattern formed over the first semiconductor pattern at another side of the first etch stop layer;

a first source electrode formed over the second semiconductor pattern, the first source electrode extending from the data bus line; and

a first drain electrode formed over the third semiconductor pattern;

a driving transistor electrically connected to the power supply line, the driving transistor comprising:

a second gate electrode electrically connected to the first drain electrode of the switching transistor;

a fourth semiconductor pattern formed over the second gate electrode;

a second etch stop layer formed over the fourth semiconductor pattern;

a fifth semiconductor pattern formed over the fourth semiconductor pattern at one side of the second etch stop layer;

a sixth semiconductor pattern formed over the fourth semiconductor pattern at another side of the second etch stop layer;

a second source electrode formed over the fifth semiconductor layer, the second source electrode extending from the power supply line; and

a second drain electrode formed over the sixth semiconductor layer;

an electro-luminescence element electrically connected to the second drain electrode of the driving transistor.

6. The electro-luminescence device of claim 5, wherein the electro-luminescence element comprises:

an anode electrode electrically connected to the second drain electrode of the driving transistor;

a light emitting layer formed over the anode electrode; and

a cathode electrode formed over the light emitting layer.

7. The electro-luminescence device of claim 6, wherein the light emitting layer is an organic light emitting layer.

8. The electro-luminescence device of claim 5, wherein the first and fourth semiconductor patterns are formed of an amorphous silicon film.

9. The electro-luminescence device of claim 5, wherein the second, third, fifth and sixth semiconductor patterns are formed of an n^+ amorphous silicon film.

10. The electro-luminescence device of claim 5, wherein the first and second etch stop layers have a thickness of about 100 Å to about 200 Å.

11. The electro-luminescence device of claim 5, further comprising:

a connecting electrode that connects the first drain electrode to the second gate electrode.

12. A method of forming an electro-luminescence device, comprising:

forming a gate bus line extending in a first direction over a substrate;

forming a data bus line extending in a second direction over the substrate;

forming a power supply line extending parallel to the data bus line over the substrate;

forming a switching transistor electrically connected to the gate bus line, the step of forming a switching transistor comprising:

forming a first gate electrode extending from the gate bus line;

forming a first semiconductor pattern over the first gate electrode;

forming a first etch stop pattern over the first semiconductor pattern;

forming a second semiconductor pattern over the first semiconductor pattern at one side of the first etch stop pattern;

forming a third semiconductor pattern over the first semiconductor pattern at another side of the first etch stop pattern;

forming a first source electrode over the second semiconductor pattern, the first source electrode extending from the data bus line; and

forming a first drain electrode over the third semiconductor pattern;

forming a driving transistor electrically connected to the power supply line, the step of forming a driving transistor comprising:

forming a second gate electrode electrically connected to the first drain electrode of the switching transistor;

forming a fourth semiconductor pattern over the second gate electrode;

forming a second etch stop pattern over the fourth semiconductor pattern;

forming a fifth semiconductor pattern over the fourth semiconductor pattern at one side of the second etch stop pattern;

forming a sixth semiconductor pattern over the fourth semiconductor pattern at another side of the second etch stop pattern;

forming a second source electrode over the fifth semiconductor layer, the second source electrode extending from the power supply line; and

forming a second drain electrode over the sixth semiconductor layer; and

forming an electro-luminescence element electrically connected to the second drain electrode of the driving transistor.

13. The method of claim 12, wherein the gate bus line, the first gate electrode and the second gate electrode are formed simultaneously by etching a gate metal thin layer.

14. The method of claim 12, wherein the first and second etch stop patterns are formed simultaneously by etching an etch stop layer.

15. The method of claim 12, wherein the data bus line, the power supply line, the first and second drain electrodes, and the first and second source electrodes are formed simultaneously by etching a source/drain metal thin layer formed over first and second semiconductor layers.

16. The method of claim 15, wherein the first, second, third, fourth, fifth and sixth semiconductor patterns are formed simultaneously by etching the first and second semiconductor layers using the data bus line, the power supply line, the first and second drain electrodes and the first and second source electrodes as a mask, and the first and second etch stop patterns prevent portions of the first and second semiconductor layers from being etched.

17. The method of claim 12, further comprising:

forming a first inter-insulating layer over the switching transistor and the driving transistor; and

forming a first, second and third contact hole in the first inter-insulating layer, the first contact hole partially exposing the first drain electrode, the second contact hole partially exposing the second gate electrode and the third contact hole partially exposing the second drain electrode.

18. The method of claim 17, further comprising:

forming an anode thin layer over the first inter-insulating layer;

forming an anode electrode of the electro-luminescence element and a connecting electrode that electrically connects the first drain electrode to the second gate electrode by etching the anode thin layer.

19. The method of claim 18, further comprising:

forming a second inter-insulating layer over the first inter-insulating layer;

forming an opening in the second inter-insulating layer that exposes the anode electrode.

20. The method of claim 18, further comprising:

forming a light-emitting layer of the electro-luminescence element over the anode electrode; and

forming a cathode electrode of the electro-luminescence element over the light-emitting layer.

21. The method of claim 20, wherein the light-emitting layer is an organic light-emitting layer.

22. A method of forming an electro-luminescence device, comprising:

forming an electro-luminescence element; and

forming a thin film transistor electrically connected to the electro-luminescence element, the step of forming a thin film transistor comprising:

forming a gate electrode over a substrate;

forming an insulating layer over the gate electrode;

forming a first semiconductor pattern over the insulating layer;

forming an etch stop pattern over the first semiconductor layer;

forming a second semiconductor pattern over the etch stop layer at one side of the etch stop pattern;

forming a third semiconductor pattern over the etch stop layer at another side of the etch stop pattern;

forming a source electrode over the second semiconductor pattern; and

forming a drain electrode over the third semiconductor pattern.

23. The method of claim 22, wherein the data bus line, the power supply line, the drain electrode, and the source electrode are formed simultaneously by etching a source/drain metal thin layer formed over first and second semiconductor layers.

24. The method of claim 23, wherein the first, second and third semiconductor patterns are formed simultaneously by etching the first and second semiconductor layers using the data bus line, the power supply line, the drain electrode and the source electrode as a mask, and the etch stop pattern prevents portions of the first semiconductor layer from being etched.